REMARKS

Claims 1-10 are pending in this application after this Amendment. Claims 1 and 5 are independent. In light of the amendments and remarks made herein, Applicants respectfully request reconsideration and withdrawal of the outstanding rejections.

In the outstanding Official Action, the Examiner rejected claims 1 and 2 under 35 U.S.C. §§ 102(a) and (b) as being anticipated by *Yamasaki et al.* (USP 5,539,916); and rejected claim 5 under 35 U.S.C. §§ 102(a) and (b) as being anticipated by *Tsuboi et al.* (USP 5,140,582). Applicants respectfully traverse these rejections.

Examiner Interview

Applicants wish to thank the Examiner for the interview conducted on November 3, 2004. During the interview, the parties discussed the prior art rejections of claims 1 and 5. The Examiner indicated he will formally consider Applicants' arguments upon receipt of Applicants' Reply.

Claim Rejections - 35 U.S.C. § 102 - *Yamasaki et al.*

In support of the Examiner's rejection of claim 1, the Examiner asserts that *Yamasaki et al.* discloses the pulse control circuit receiving one data transfer request pulse signal as the first pulse from the transfer control circuit in the preceding stage to output a plurality of data transfer request pulse signals as the second pulse to the transfer control circuit in the

subsequent stage, citing to the BRQ pulse signals in Figs. 2 and 4. Applicants respectfully disagree with the Examiner's characterization of this reference.

As discussed during the interview, *Yamasaki et al.* discloses at col. 3, lines 26-35 as follows:

> The operation of the DMA control system will be described with respect to FIG. 2. First of all, a DMA request signal DRQ (No. 1) is outputted by one of the I/O devices 12a for requesting a DMA transfer. This DMA request signal DRQ is applied to the transfer pulse generator 11 via the OR gate 13. The transfer pulse generator 11 detects the falling edge and outputs a request pulse p to the request signal generator 10. The request pulse p triggers the request signal generator 10 to output a positive logic bus request signal BRQ to the bus access controller 14.

As can be seen from the above teachings, *Yamasaki et al.* merely discloses outputting one positive logic bus request signal BRQ based upon a DMA request signal output by one of the I/O devices 12a.

In contrast, the present invention as set forth in claim 1 recites, *inter alia*, a pulse control circuit receiving one data transfer request pulse signal to output a plurality of data transfer request pulse signals. As *Yamasaki et al.* fails to teach or suggest outputting a plurality of data transfer request pulse signals when receiving one data transfer request pulse signal, it is respectfully submitted that *Yamasaki et al.* fails to anticipate

the present invention. As such, it is respectfully requested that the outstanding rejection be withdrawn.

It is respectfully submitted that claim 2 is allowable for the reasons set forth above with regard to claim 1 at least based upon its dependency on claim 1.

Claim Rejections - 35 U.S.C. § 102 - *Tsuboi et al.*

In support of the Examiner's rejection of claim 5, the Examiner asserts that *Tsuboi et al.* discloses a data transmission path holding a data packet based on a pulse signal applied from a self-synchronous transfer control circuit. The Examiner asserts that, although *Tsuboi et al.* does not explicitly teach this claim element, the *Tsuboi et al.* system inherently discloses this claim element. The Examiner further cites to successive packets being written into buffer 31 as recited in col. 23, lines 40-53. The Examiner further asserts that *Tsuboi et al.* discloses the counter of the present invention, citing to counter 38. Applicants respectfully disagree with the Examiner's characterization of this reference.

As described in *Tsuboi* at col. 13, lines 29-43, the controllers are synchronized with the clock circuit 34. The "pulse" signal as claimed could not be interpreted as a clock signal. Self-synchronous systems use communication signals that are shared among elements in the system, i.e., the CI, RO, CO, and RI signals of the present invention. As such, *Tsuboi* fails to teach a self-

synchronous system that holding a data packet based on a pulse signal applied from the self-synchronous transfer control circuit.

Tsuboi further fails to teach the data number detection means and the self-synchronous transfer control circuit outputting a transfer request pulse signal corresponding to the number of data in response to detection of the number of data by the data number detection means. The Examiner relies on counter 38 as described with respect to Fig. 17. However, this counter does not perform the same functionality as the data number detection means as claimed. The counter of *Tsuboi* at col. 23, lines 40-53 is described as follows:

> This counter 38 divides the packet information for every predetermined length (corresponding to the aforementioned time length T.). The divided packets are successively written into the receive packet buffer 31. During this operation, the packet division number counter 38 counts the number of divided packet frames (division number, or the number of packet frames by which the input packet is transferred). The length of each packet frame corresponding to the time length T is determined so that the entire transfer request frame consisting of the status information, the transfer request information, the requested packet frame number information and the continuation information is less than the transfer period T.

Based upon the above teaching, the counter of *Tsuboi* merely divides packets to ensure all of the information is transferred within the transfer period. However, the data number detection means of the present invention detects the number of data based on

output packet information set to the data packet held in the data transmission path.

Based upon the reasons set forth above, it is respectfully submitted that claim 5 is not anticipated by the teachings of *Tsuboi et al*. It is respectfully requested that the outstanding rejection be withdrawn.

It is respectfully submitted that new dependent claim 9 is allowable for the reasons set forth above with regard to claim 5 at least based upon its dependency on claim 5.

Conclusion

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Catherine M. Voisinet (Reg. No. 52,327) at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

Applicants respectfully petition for a one (1) month extension of time pursuant to 37 C.F.R. §§ 1.17 and 1.136(a). A check in the amount of $110.00 in payment of the extension of time fee is attached.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees

required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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